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NO. 4416 P. 1/6

**MAY 23 2005**

**PATENT**  
**5298-08101/PM01039D**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:  
Ramkumar et al.

Serial No.: 10/740,205

Filed: December 18, 2003

For: **SONOS STRUCTURE INCLUDING  
A DEUTEREATED OXIDE-SILICON  
INTERFACE AND METHOD FOR  
MAKING THE SAME**

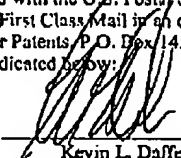
Group Art Unit: 2814

Examiner: Pham, H.

Atty. Dkt. No.: 5298-08101

I hereby certify that this correspondence is being transmitted via facsimile or deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313, on the date indicated below:

May 23, 2005  
Date

  
Kevin L. Daffer

**DECLARATION UNDER 37 C.F.R. § 1.131**

Commissioner for Patents  
Washington, D.C. 20231

I, Krishnaswamy Ramkumar, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 10/740,205 filed on December 18, 2003, a divisional application of parent U.S. Patent Application No. 10/094,108 filed on May 8, 2002.
2. I have been informed that in the present application certain claims have been rejected in reference to U.S. Patent No. 6,661,065 to Kunikiyo, which was issued on December 9, 2003, was first published on April 25, 2002, and was filed on February 13, 2001.

### CONCEPTION

3. As supported below, I, along with Frederick B. Jenne, conceived of the subject matter claimed in the present application within the United States before February 13, 2001. The subject matter includes a semiconductor topography including a silicon-oxide-nitride-oxide-silicon (SONOS) structure and a nitride layer comprising deuterium arranged above the SONOS structure.

4. Exhibit A attached hereto is a true copy of a memorandum which bears a date before February 13, 2001 corresponding to the conception of the invention. The actual date of the memorandum has been redacted.

5. Pages 2 and 3 of Exhibit A describe the subject matter of the presently claimed case including a semiconductor topography with a SONOS structure having a nitride layer formed using deuterium and a SAC (self aligned contact) nitride layer formed using deuterium.

### REDUCTION TO PRACTICE AND DILIGENCE

6. From at least a time just prior to February 13, 2001 through the filing of parent U.S. Patent Application No. 10/094,108 filed on May 8, 2002, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley Rose, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to February 13, 2001 through the filing of the parent application on May 8, 2002.

7. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to February 13, 2001 through the filing of the parent application on May 8, 2002.

8. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these

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NO. 4416 P. 3/6

statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Krishnaswamy Ramkumar  
Krishnaswamy Ramkumar  
Date: 4/11/05